

# LP2989 Micropower and Low-Noise, 500-mA Ultra Low-Dropout Regulator for Use With Ceramic Output Capacitors

## 1 Features

- 2.1 V to 30 V Input Voltage Range
- 2.5 V to 5 V Fixed Output Voltage Options
- Ultra-Low Dropout Voltage
- Specified 500-mA Continuous Output Current
- Very Low Output Noise With External Capacitor
- SO-8, Mini SO-8, 8 Lead LLP Surface Mount Packages
- < 0.8- $\mu$ A Quiescent Current When Shutdown
- Low Ground Pin Current at All Loads
- 0.75% Output Voltage Accuracy (A Grade)
- High Peak Current Capability (800 mA typical)
- Wide Supply Voltage Range (16 V Max)
- Overtemperature and Overcurrent Protection
- -40°C to 125°C Junction Temperature Range

## 2 Applications

- Notebooks and Desktop PCs
- PDAs and Palmtop Computers
- Wireless Communication Pins
- SMPS Post-Regulators

## 3 Description

The LP2989 is a fixed-output 500-mA precision LDO regulator designed for use with ceramic output capacitors.

Output noise can be reduced to 18  $\mu$ V (typical) by connecting an external 10-nF capacitor to the bypass pin.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2989 delivers superior performance:

- **Dropout Voltage:** Typically 310 mV at 500-mA load, and 1 mV at 100- $\mu$ A load.
- **Ground Pin Current:** Typically 3 mA at 500-mA load, and 110  $\mu$ A at 100- $\mu$ A load.
- **Sleep Mode:** The LP2989 draws less than 0.8- $\mu$ A quiescent current when SHUTDOWN pin is pulled low.
- **Error Flag:** The built-in error flag goes low when the output drops approximately 5% below nominal.
- **Precision Output:** Specified output voltage accuracy is 0.75% (A grade) and 1.25% (standard grade) at room temperature.

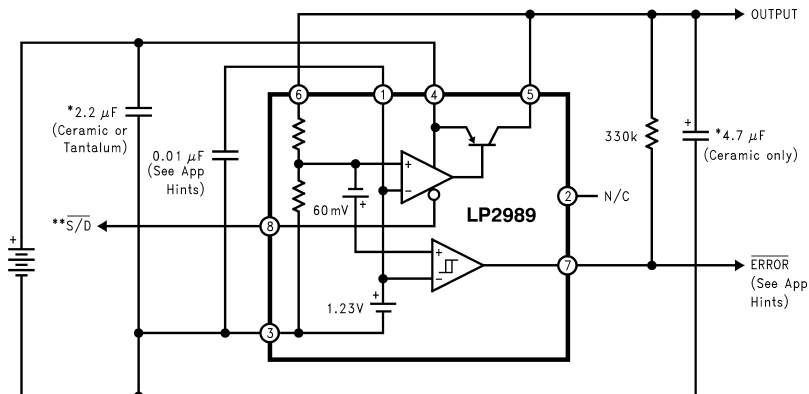
For output voltages < 2 V, see LP2989LV ([SNVS806](#)) data sheet.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2989	WSON (8)	4.00 mm x 4.00 mm
	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Basic Application Circuit



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## 4 Revision History

### Changes from Revision M (February 2005) to Revision N

**Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... **1**

## 5 Output Voltage Options

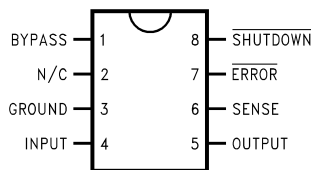
ORDER NUMBER	OUTPUT VOLTAGE OPTION (V) <sup>(1)</sup>	GRADE
<b>8-LEAD LLP</b>		
LP2989AILD	2.5	A
LP2989AILD	2.5	A
LP2989ILD	2.5	STD
LP2989ILD	2.5	STD
LP2989AILD	2.8	A
LP2989AILD	2.8	A
LP2989ILD	2.8	STD
LP2989ILD	2.8	STD
LP2989AILD	2.85	A
LP2989AILD	2.85	A
LP2989ILD	2.85	STD
LP2989ILD	2.85	STD
LP2989AILD	3	A
LP2989AILD	3	A
LP2989ILD	3	STD
LP2989ILD	3	STD
LP2989AILD	3.3	A
LP2989AILD	3.3	A
LP2989ILD	3.3	STD
LP2989ILD	3.3	STD
LP2989AILD	3.6	A
LP2989AILD	3.6	A
LP2989ILD	3.6	STD
LP2989ILD	3.6	STD
LP2989AILD	4	A
LP2989AILD	4	A
LP2989ILD	4	STD
LP2989ILD	4	STD
LP2989AILD	5	A
LP2989AILD	5	A
LP2989ILD	5	STD
LP2989ILD	5	STD
<b>8-LEAD MSOP (MM)</b>		
LP2989AIMM	2.5	A
LP2989AIMM	2.5	A
LP2989IMM	2.5	STD
LP2989IMM	2.5	STD
LP2989AIMM	2.8	A
LP2989AIMM	2.8	A
LP2989IMM	2.8	STD
LP2989IMM	2.8	STD
LP2989AIMM	3	A
LP2989AIMM	3	A
LP2989IMM	3	STD

(1) For output voltages < 2 V, see LP2989LV (SNVS806) datasheet.

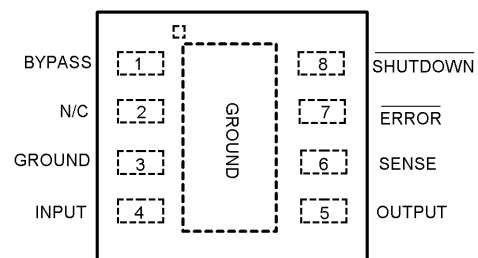
ORDER NUMBER	OUTPUT VOLTAGE OPTION (V) <sup>(1)</sup>	GRADE
LP2989IMMX	3	STD
LP2989AIMM	3.3	A
LP2989AIMMX	3.3	A
LP2989IMM	3.3	STD
LP2989IMMX	3.3	STD
LP2989AIMM	5	A
LP2989AIMMX	5	A
LP2989IMM	5	STD
LP2989IMMX	5	STD
<b>SO-8 (M)</b>		
LP2989AIMX	2.5	A
LP2989AIM	2.5	A
LP2989IMX	2.5	STD
LP2989IM	2.5	STD
LP2989AIMX	3	A
LP2989AIM	3	A
LP2989IMX	3	STD
LP2989IM	3	STD
LP2989AIMX	3.3	A
LP2989AIM	3.3	A
LP2989IMX	3.3	STD
LP2989IM	3.3	STD
LP2989AIMX	5	A
LP2989AIM	5	A
LP2989IMX	5	STD
LP2989IM	5	STD

## 6 Pin Configuration and Functions

**8-Pin SO/Mini Package**  
**Package Numbers M08A/MUA08A**  
**Top View**



**8-Lead LLP**  
**Package Number LDC08A**  
**Top View**



## Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BYPASS	1	I	Bypass capacitor input
/ERROR	7	O	Error signal output
GROUND	3	—	GND
INPUT	4	I	Regulator power input
N/C	2	—	NC
OUTPUT	5	O	Regulated output voltage
SENSE	6	I	Feedback voltage sense input
/SHUTDOWN	8	I	Shutdown input

## 7 Specifications

### 7.1 Absolute Maximum Ratings

If Military/Aerospace specified devices are required contact the National Semiconductor Sales Office/Distributors for availability and specifications.<sup>(1)</sup>

		MIN	MAX	UNIT
Operating junction temperature range		–40	125	°C
Power dissipation <sup>(2)</sup>		Internally Limited		
Input supply voltage	Survival	–0.3	16	V
	Operating	2.1	16	V
Sense pin		–0.3	6	V
Output voltage	Survival <sup>(3)</sup>	–0.3	16	V
I <sub>OUT</sub> (Survival)		Short Circuit Protected		
Input-Output voltage	Survival <sup>(4)</sup>	–0.3	16	V
Storage temperature range, T <sub>stg</sub>		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P(\text{MAX}) = \frac{T_J(\text{MAX}) - T_A}{\theta_{JA}}$$

The value of θ<sub>JA</sub> for the SO-8 (M) package is 160°C/W and the mini SO-8 (MM) package is 200°C/W. The value θ<sub>JA</sub> for the LLP (LD) package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

(3) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2989 output must be diode-clamped to ground.

(4) The output PNP structure contains a diode between the V<sub>IN</sub> and V<sub>OUT</sub> pins that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000 V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating junction temperature range	-40	125	°C
Operating Input supply voltage	2.1	1.6	V

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LP2989			UNIT
		NGN	D	DGK	
		8 PINS	8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	34.8	114.5	156.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	28.4	61.1	51.0	
R <sub>θJB</sub>	Junction-to-board thermal resistance	12.0	55.6	76.5	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	9.7	4.9	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	12.2	54.9	75.2	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	1.3	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

### 7.5 Electrical Characteristics

Unless otherwise specified: T<sub>J</sub> = 25°C, V<sub>IN</sub> = V<sub>O(NOM)</sub> + 1 V, I<sub>L</sub> = 1 mA, C<sub>OUT</sub> = 4.7 μF, C<sub>IN</sub> = 2.2 μF, V<sub>SD</sub> = 2 V.

PARAMETER	TEST CONDITIONS	LP2989AI-X.X <sup>(1)</sup>			LP2989I-X.X <sup>(1)</sup>			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>O</sub>	Output voltage tolerance		-0.75	0.75	-1.25	1.25	%V <sub>NOM</sub>	
		1 mA < I <sub>L</sub> < 500 mA, V <sub>O(NOM)</sub> + 1 V ≤ V <sub>IN</sub> ≤ 16 V	-1.5	1.5	-2.5	2.5		
		1 mA < I <sub>L</sub> < 500 mA, V <sub>O(NOM)</sub> + 1 V ≤ V <sub>IN</sub> ≤ 16 V, -40°C ≤ T <sub>J</sub> ≤ 125°C	-4.0	2.5	-5.0	3.5		
		1 mA < I <sub>L</sub> < 500 mA, V <sub>O(NOM)</sub> + 1 V ≤ V <sub>IN</sub> ≤ 16 V, -25°C ≤ T <sub>J</sub> ≤ 125°C	-3.5	2.5	-4.5	3.5		
$\frac{\Delta V_O}{\Delta V_{IN}}$	Output voltage line regulation	V <sub>O(NOM)</sub> + 1 V ≤ V <sub>IN</sub> ≤ 16 V	0.005	0.014	0.005	0.014	%V	
		V <sub>O(NOM)</sub> + 1 V ≤ V <sub>IN</sub> ≤ 16 V, -40°C ≤ T <sub>J</sub> ≤ 125°C	0.005	0.032	0.005	0.032		
$\frac{\Delta V_O}{\Delta I_L}$	Load regulation	1 mA < I <sub>L</sub> < 500 mA	0.4		0.4		%V <sub>NOM</sub>	
V <sub>IN</sub> -V <sub>O</sub>	Dropout voltage <sup>(2)</sup>	I <sub>L</sub> = 100 μA	1	3	1	3	mV	
		I <sub>L</sub> = 100 μA, -40°C ≤ T <sub>J</sub> ≤ 125°C	1	4	1	4		
		I <sub>L</sub> = 200 mA	150	200	150	200	mV	
		I <sub>L</sub> = 200 mA, -40°C ≤ T <sub>J</sub> ≤ 125°C	150	300	150	300		
		I <sub>L</sub> = 500 mA	310	425	310	425	mV	
		I <sub>L</sub> = 500 mA, -40°C ≤ T <sub>J</sub> ≤ 125°C	310	650	310	650		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

(2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1 V differential.

**Electrical Characteristics (continued)**

Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_O(\text{NOM}) + 1\text{ V}$ ,  $I_L = 1\text{ mA}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ ,  $C_{IN} = 2.2\text{ }\mu\text{F}$ ,  $V_{S/D} = 2\text{ V}$ .

PARAMETER	TEST CONDITIONS	LP2989AI-X.X <sup>(1)</sup>			LP2989I-X.X <sup>(1)</sup>			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$I_{GND}$ Ground pin current	$I_L = 100\text{ }\mu\text{A}$		110	175		110	175	$\mu\text{A}$
	$I_L = 100\text{ }\mu\text{A}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		110	200		110	200	
	$I_L = 200\text{ mA}$		1	2		1	2	mA
	$I_L = 200\text{ mA}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		1	3.5		1	3.5	
	$I_L = 500\text{ mA}$		3	6		3	6	mA
	$I_L = 500\text{ mA}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		3	9		3	9	
	$V_{S/D} < 0.18\text{ V}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		0.5	2		0.5	2	$\mu\text{A}$
$V_{S/D} < 0.4\text{ V}$		0.05	0.8		0.05	0.8		
$I_O(\text{PK})$ Peak output current	$V_{OUT} \geq V_O(\text{NOM}) - 5\%$	600	800		600	800		mA
$I_O(\text{MAX})$ Short circuit current	$R_L = 0$ (Steady State) <sup>(3)</sup>		1000			1000		mA
$e_n$ Output noise voltage (RMS)	BW = 100 Hz to 100 kHz, $C_{OUT} = 10\text{ }\mu\text{F}$ , $C_{BYPASS} = .01\text{ }\mu\text{F}$ , $V_{OUT} = 2.5\text{ V}$		18			18		$\mu\text{V}(\text{RMS})$
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$ Ripple Rejection	$f = 1\text{ kHz}$ , $C_{OUT} = 10\text{ }\mu\text{F}$		60			60		dB
$\frac{\Delta V_{OUT}}{\Delta T}$ Output voltage temperature coefficient	See <sup>(4)</sup> , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		20			20		ppm/ $^\circ\text{C}$
<b>SHUTDOWN INPUT</b>								
$V_{S/D}$ S/D Input voltage	$V_H = \text{O/P ON}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	1.6	1.4		1.6	1.4		V
	$V_L = \text{O/P OFF}$ , $I_{IN} \leq 2\text{ }\mu\text{A}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		0.50	0.18		0.50	0.18	
$I_{S/D}$ S/D Input current	$V_{S/D} = 0$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		0.001	-1		0.001	-1	$\mu\text{A}$
	$V_{S/D} = 5\text{ V}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		5	15		5	15	
<b>ERROR COMPARATOR</b>								
$I_{OH}$ Output "HIGH" leakage	$V_{OH} = 16\text{ V}$		0.001	1		0.001	1	$\mu\text{A}$
	$V_{OH} = 16\text{ V}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		0.001	2		0.001	2	
$V_{OL}$ Output "LOW" voltage	$V_{IN} = V_O(\text{NOM}) - 0.5\text{ V}$ , $I_O(\text{COMP}) = 150\text{ }\mu\text{A}$		150	220		150	220	mV
	$V_{IN} = V_O(\text{NOM}) - 0.5\text{ V}$ , $I_O(\text{COMP}) = 150\text{ }\mu\text{A}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		150	350		150	350	
$V_{THR}(\text{MAX})$ Upper threshold voltage		-6.0	-4.8	-3.5	-6.0	-4.8	-3.5	% $V_{OUT}$
	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	-8.3	-4.8	-2.5	-8.3	-4.8	-2.5	
$V_{THR}(\text{MIN})$ Lower threshold voltage		-8.9	-6.6	-4.9	-8.9	-6.6	-4.9	% $V_{OUT}$
	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	-13.0	-6.6	-3.0	-13.0	-6.6	-3.0	
HYST Hysteresis			2			2		% $V_{OUT}$

<sup>(3)</sup> See the [Typical Characteristics](#) section.

<sup>(4)</sup> Temperature coefficient is defined as the maximum (worst-case) change divided by the total temperature range.

### 7.6 Typical Characteristics

$T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1 \text{ V}$ ,  $I_L = 1 \text{ mA}$ ,  $V_{OUT} = 2.5 \text{ V}$  (unless otherwise specified)

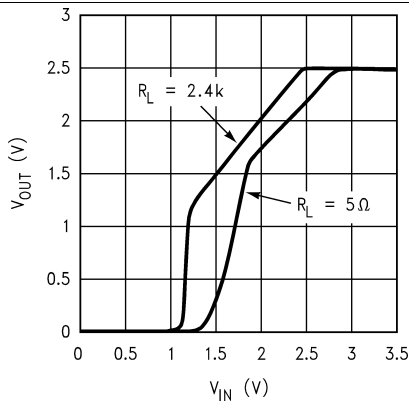


Figure 1. Dropout Characteristics

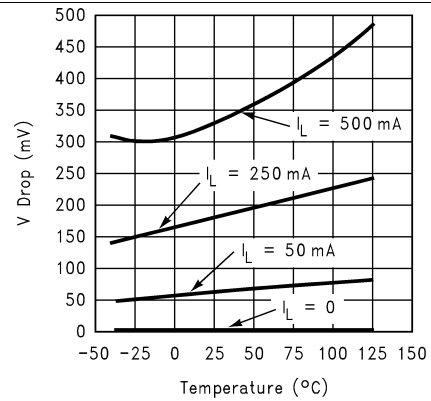


Figure 2. Dropout Voltage vs Temperature

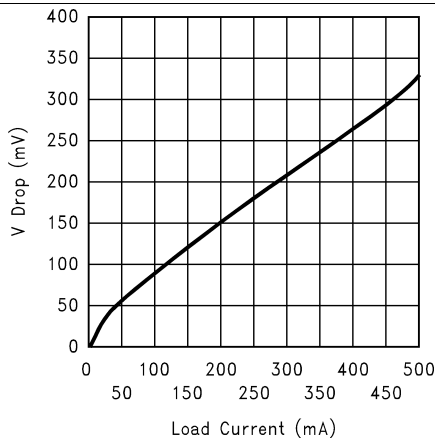


Figure 3. Dropout Voltage vs Load Current

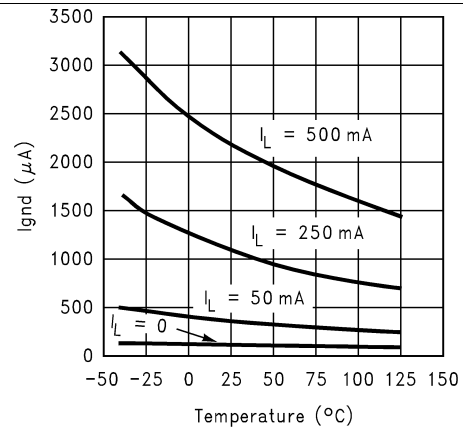


Figure 4. GND Pin Current vs Temperature and Load

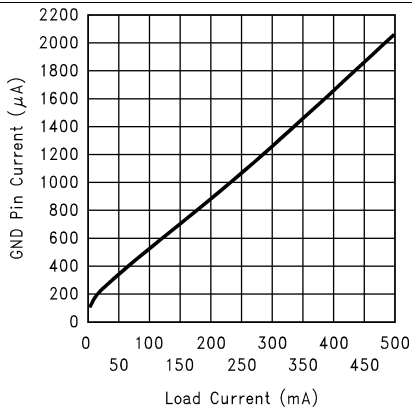


Figure 5. Ground Pin Current vs Load Current

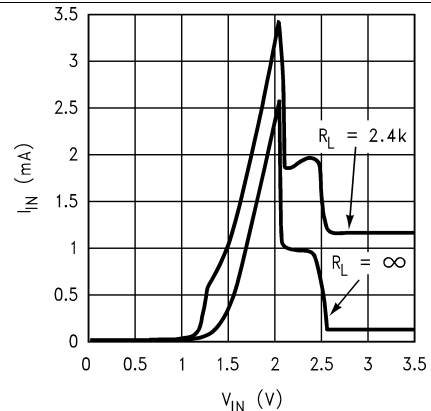
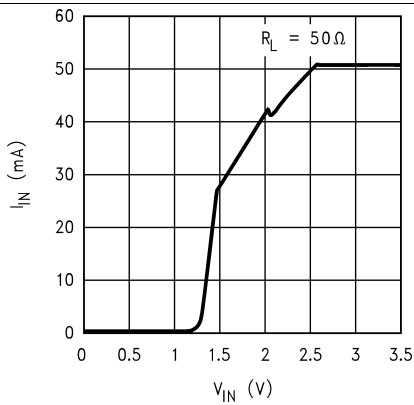


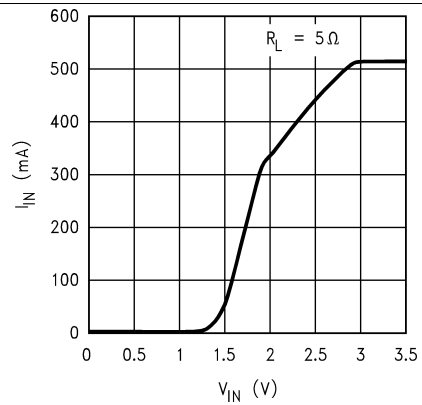
Figure 6. Input Current vs  $V_{IN}$

**Typical Characteristics (continued)**

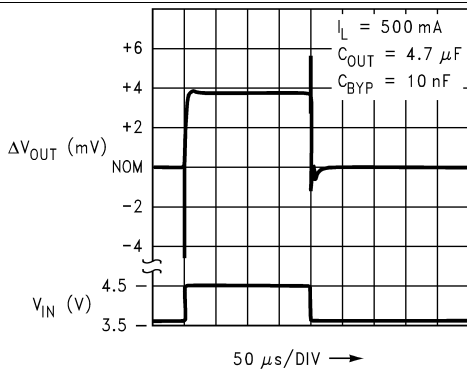
$T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1 \text{ V}$ ,  $I_L = 1 \text{ mA}$ ,  $V_{OUT} = 2.5 \text{ V}$  (unless otherwise specified)



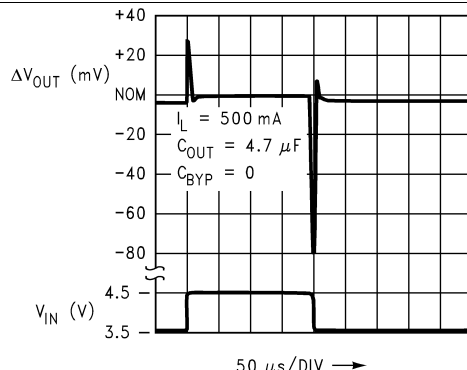
**Figure 7. Input Current vs  $V_{IN}$**



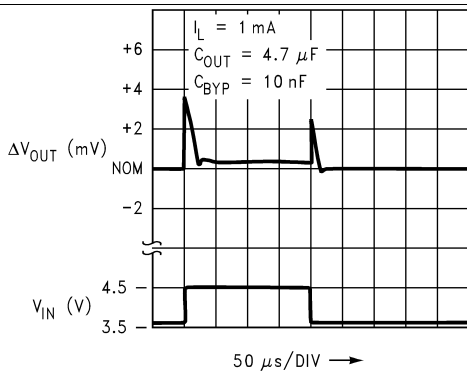
**Figure 8. Input Current vs  $V_{IN}$**



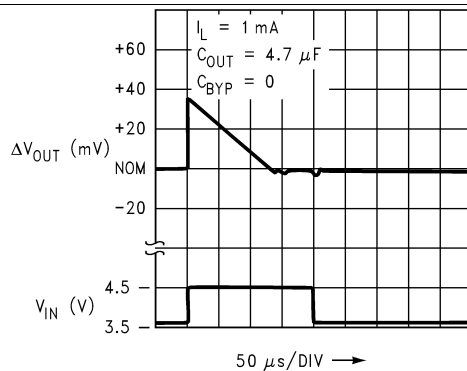
**Figure 9. Line Transient Response**



**Figure 10. Line Transient Response**



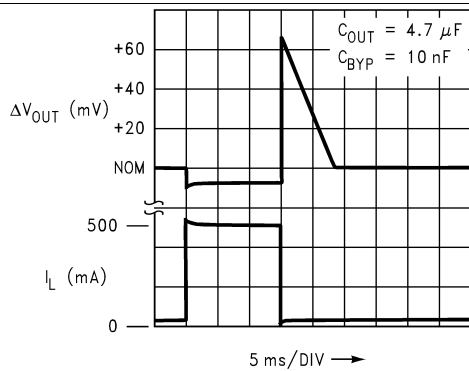
**Figure 11. Line Transient Response**



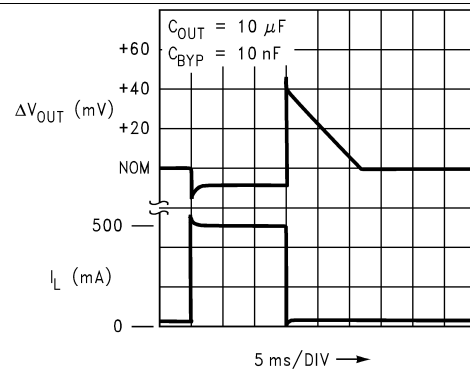
**Figure 12. Line Transient Response**

**Typical Characteristics (continued)**

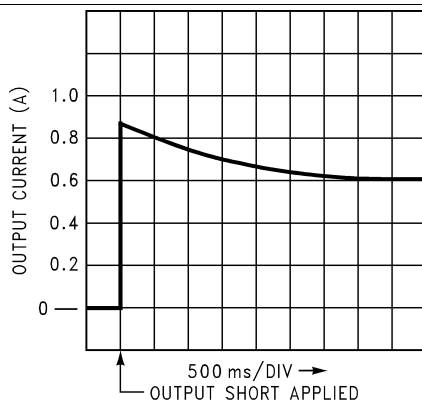
$T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1 \text{ V}$ ,  $I_L = 1 \text{ mA}$ ,  $V_{OUT} = 2.5 \text{ V}$  (unless otherwise specified)



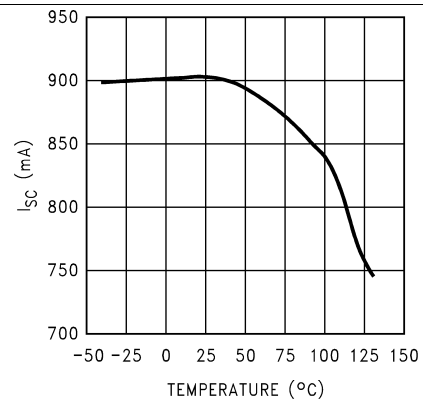
**Figure 13. Load Transient Response**



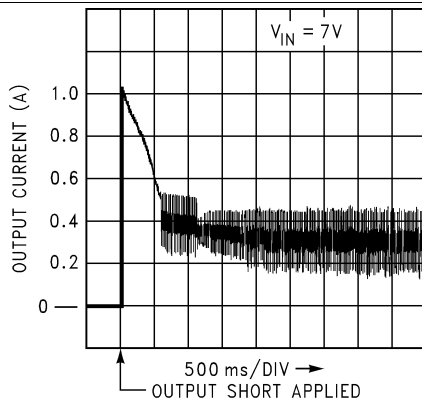
**Figure 14. Load Transient Response**



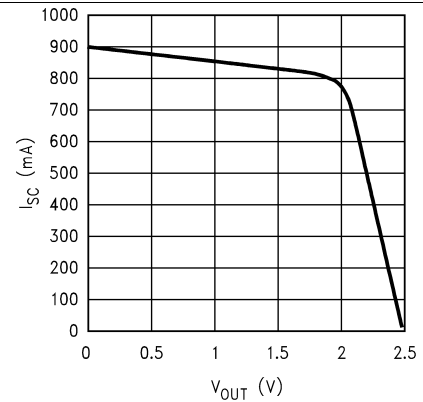
**Figure 15. Short Circuit Current**



**Figure 16. Short Circuit Current vs Temperature**



**Figure 17. Short Circuit Current**



**Figure 18. Short Circuit Current vs  $V_{OUT}$**

**Typical Characteristics (continued)**

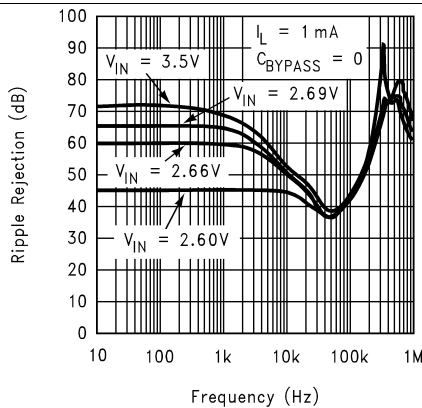
$T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1 \text{ V}$ ,  $I_L = 1 \text{ mA}$ ,  $V_{OUT} = 2.5 \text{ V}$  (unless otherwise specified)



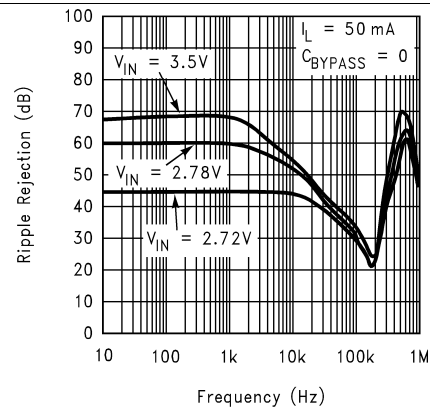
**Figure 19. Ripple Rejection**



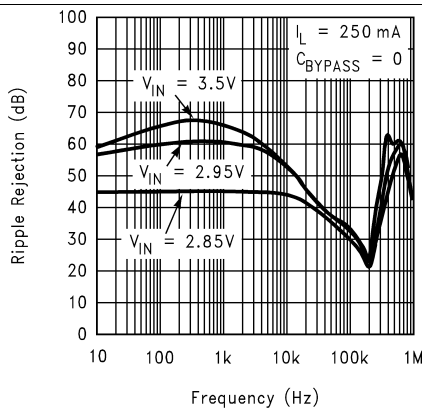
**Figure 20. Ripple Rejection**



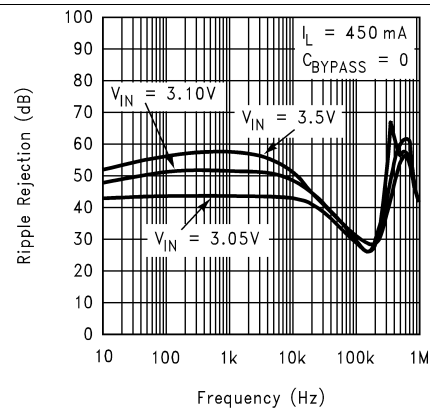
**Figure 21. Ripple Rejection**



**Figure 22. Ripple Rejection**



**Figure 23. Ripple Rejection**



**Figure 24. Ripple Rejection**

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1 \text{ V}$ ,  $I_L = 1 \text{ mA}$ ,  $V_{OUT} = 2.5 \text{ V}$  (unless otherwise specified)

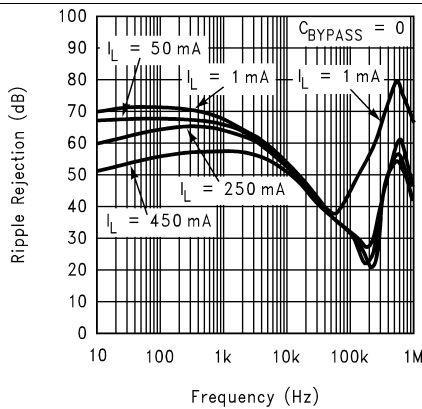


Figure 25. Ripple Rejection

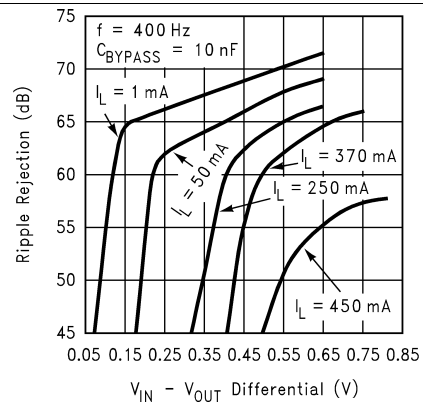


Figure 26. Ripple Rejection in Dropout

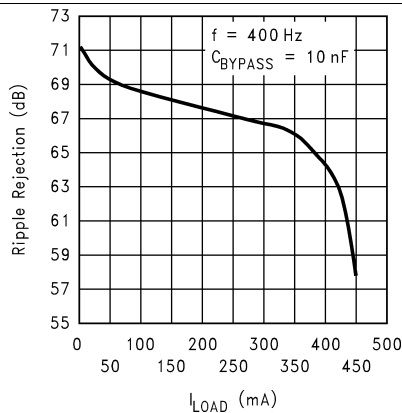


Figure 27. Ripple Rejection vs Load

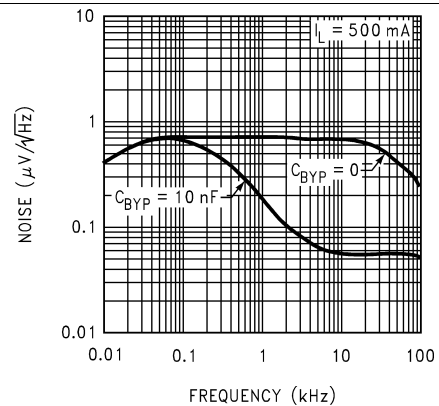


Figure 28. Output Noise Density

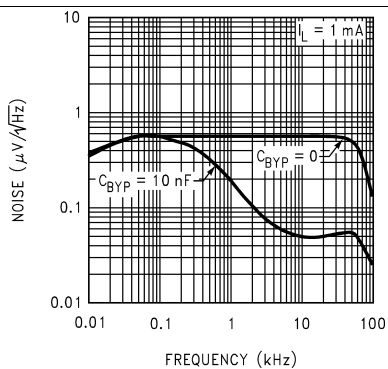


Figure 29. Output Noise Density

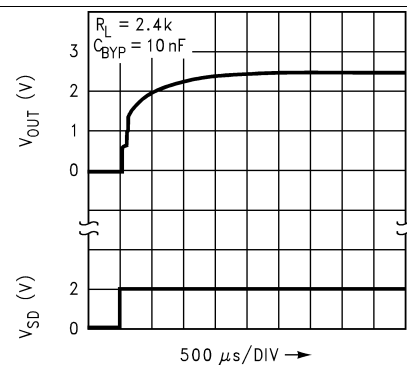
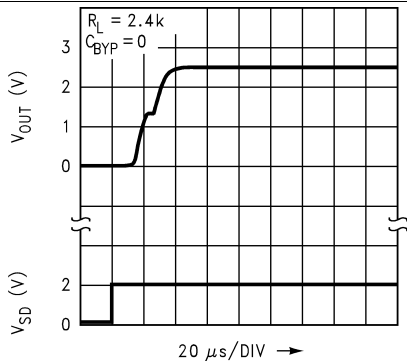


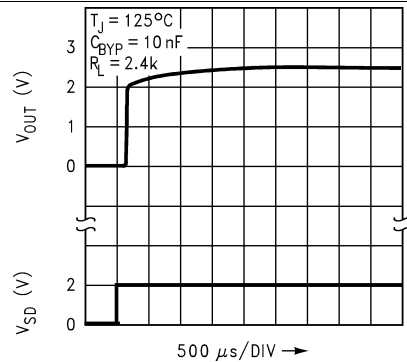
Figure 30. Turn-ON Waveform

**Typical Characteristics (continued)**

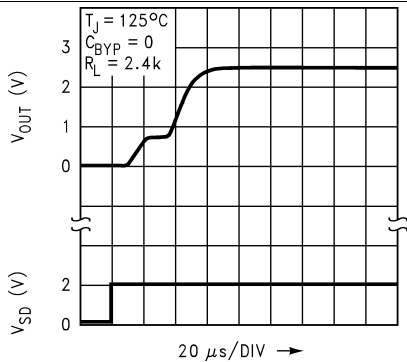
$T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7\ \mu\text{F}$ ,  $C_{IN} = 2.2\ \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1\ \text{V}$ ,  $I_L = 1\ \text{mA}$ ,  $V_{OUT} = 2.5\ \text{V}$  (unless otherwise specified)



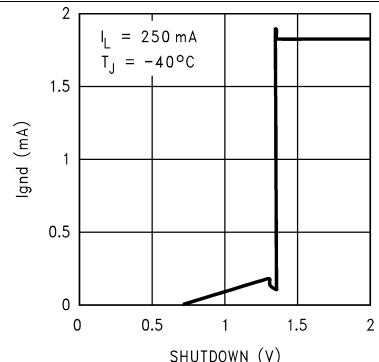
**Figure 31. Turn-ON Waveform**



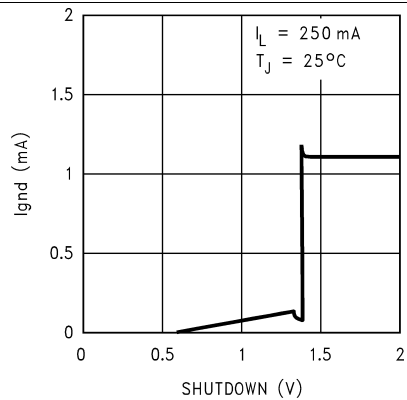
**Figure 32. Turn-ON Waveform**



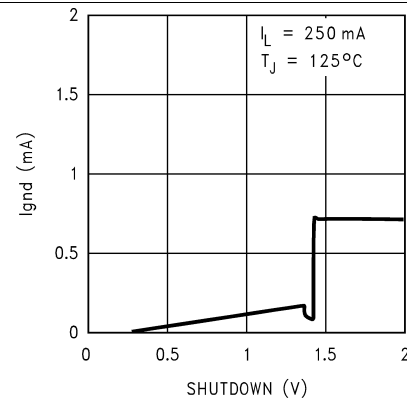
**Figure 33. Turn-ON Waveform**



**Figure 34.  $I_{GND}$  vs Shutdown**



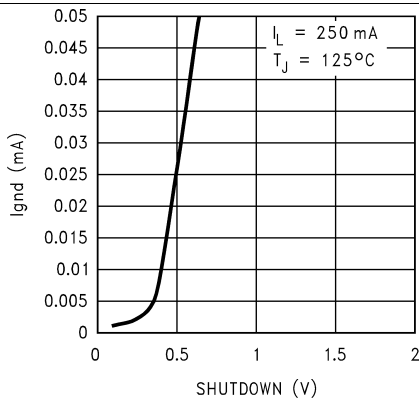
**Figure 35.  $I_{GND}$  vs Shutdown**



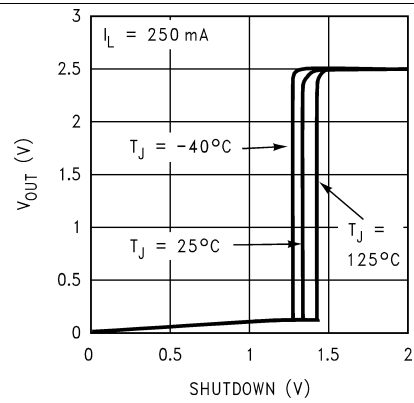
**Figure 36.  $I_{GND}$  vs Shutdown**

**Typical Characteristics (continued)**

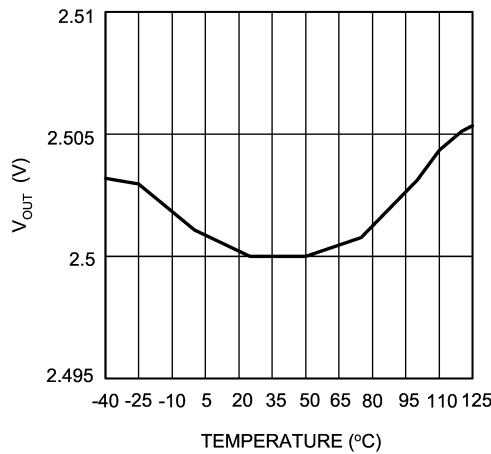
$T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1 \text{ V}$ ,  $I_L = 1 \text{ mA}$ ,  $V_{OUT} = 2.5 \text{ V}$  (unless otherwise specified)



**Figure 37.  $I_{GND}$  vs Shutdown**



**Figure 38.  $V_{OUT}$  vs Shutdown**



**Figure 39. Typical Temperature vs  $V_{OUT}$  (LP2989-2.5)**

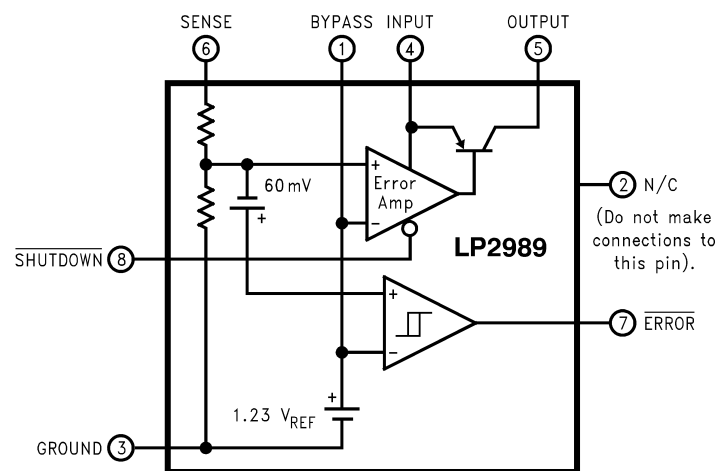
## 8 Detailed Description

### 8.1 Overview

The LP2989 are very high-accuracy micro power voltage regulators with low quiescent current (75  $\mu$ A typical) and low dropout voltage (typ. 40 mV at light loads and 380 mV at 100 mA). They are ideally suited for use in battery-powered systems. The LP2989 block diagram contains several features, including:

- Very high accuracy 1.23-V reference
- Fixed 2.5-V to 5-V versions
- Shutdown input
- Error flag output
- Internal protection circuitry, such as foldback current limit, and thermal shutdown

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 High-Accuracy Output Voltage

With special careful design to minimize all contributions to the output voltage error, the LP2989 distinguished itself as a very high output voltage accuracy micro power LDO. This includes a tight initial tolerance (.75% typical, A grade), extremely good line regulation (.005%/V typical.) and a very low output noise voltage (10  $\mu$ Vrms typical), making the part an ideal a low-power voltage reference.

#### 8.3.2 Sleep Mode

When pull SHUTDOWN pin to high level, LP2989 enters shutdown mode and a very low quiescent current is consumed. This function is designed for the application which needs a shutdown mode to effectively enhance battery life cycle.

#### 8.3.3 Error Detection Comparator Output

The LP2989 will generate a logic low output whenever its output falls out of regulation by more than approximately 5%. Refer to application information for more details.

## Feature Description (continued)

### 8.3.4 Short Circuit Protection (Current Limit)

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output. A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If OUT is forced below 0 V before EN goes high and the load current required exceeds the foldback current limit, the device may not start correctly.

### 8.3.5 Thermal Protection

The device contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced. The internal protection circuitry of the device is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability.

## 8.4 Device Functional Modes

### 8.4.1 Operation With $16\text{ V} \geq V_{IN} > V_{OUT}(\text{TARGET}) + 1.0\text{ V}$

The device operate if the input voltage is equal to, or exceeds  $V_{OUT}(\text{TARGET}) + 1.0\text{ V}$ . At input voltages below the minimum  $V_{IN}$  requirement, the devices do not operate correctly and output voltage may not reach target value.

### 8.4.2 Operation with Shutdown Control

If the voltage on the SHUTDOWN pin is less than 1.4 V, the device is disabled. Raising ON/OFF above 1.4 V initiates the start-up sequence of the device.

### 8.4.3 Capacitor Characteristics

#### 8.4.3.1 Ceramic

The LP2989 was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 4.7  $\mu\text{F}$  range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 4.7  $\mu\text{F}$  ceramic capacitor is in the range of 10 m $\Omega$  to 15 m $\Omega$ , which easily meets the ESR limits required for stability by the LP2989.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Many large-value ceramic capacitors ( $\geq 2.2\text{ }\mu\text{F}$ ) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This could cause problems if a 4.7  $\mu\text{F}$  capacitor were used on the output because it will drop down to approximately 2.4  $\mu\text{F}$  at high ambient temperatures (which could cause the LP2989 to oscillate). Another significant problem with Z5U and Y5V dielectric devices is that the capacitance drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it.

**For these reasons, X7R and X5R type ceramic capacitors must be used on the input and output of the LP2989.**

#### 8.4.3.2 Tantalum

Tantalum capacitors are less desirable than ceramics for use as output capacitors because they are typically more expensive when comparing equivalent capacitance and voltage ratings in the 1  $\mu\text{F}$  to 4.7  $\mu\text{F}$  range.

## Device Functional Modes (continued)

Another important consideration is that Tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a Tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value.

The ESR of a typical Tantalum capacitor will increase about 2:1 as the temperature falls from 25°C to -40°C, so some guard band must be allowed.

Tantalum capacitors may be used on the input as long as the requirement for minimum capacitance is met.

### 8.4.3.3 Film

Polycarbonate and polypropylene film capacitors have excellent electrical performance: their ESR is the lowest of the three types listed, their capacitance is very stable with temperature, and DC leakage current is extremely low.

One disadvantage is that film capacitors are larger in physical size than ceramic or tantalum which makes film a poor choice for either input or output capacitors.

However, their low leakage makes them a good choice for the noise bypass capacitor. Because the required amount of capacitance is only 0.01  $\mu\text{F}$ , small surface-mount film capacitors are available in this size.

### 8.4.4 Shutdown Input Operation

The LP2989 is shut off by driving the Shutdown input low, and turned on by pulling it high. If this feature is not to be used, the Shutdown input should be tied to  $V_{\text{IN}}$  to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the Shutdown input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the [Electrical Characteristics](#) section under VON/OFF.

To prevent mis-operation, the turn-on (and turn-off) voltage signals applied to the Shutdown input must have a slew rate which is  $\geq 40 \text{ mV}/\mu\text{s}$ .

#### CAUTION

The regulator output voltage **cannot** be ensured if a slow-moving AC (or DC) signal is applied that is in the range between the specified turn-on and turn-off voltages listed under the electrical specification  $V_{\text{ON/OFF}}$  (see the [Electrical Characteristics](#) table).

## 9 Application and Implementation

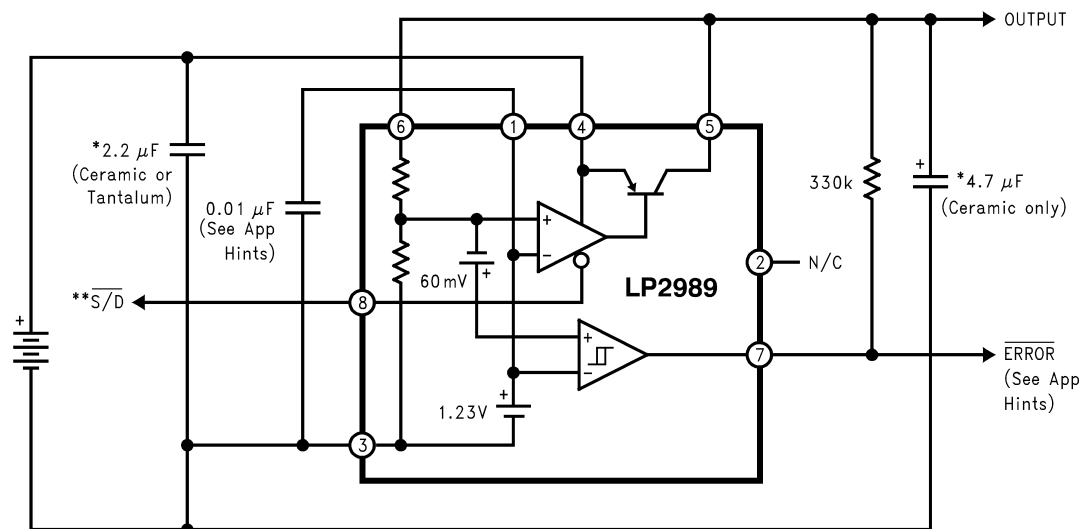
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LP2989 is a linear voltage regulator operating from 2.1 V to 16 V on the input and regulates voltages between 2.5 V to 5.0 V with 0.75% accuracy and 500 mA maximum outputs current. Efficiency is defined by the ratio of output voltage to input voltage because the LP2989 is a linear voltage regulator. To achieve high efficiency, the dropout voltage ( $V_{IN} - V_{OUT}$ ) must be as small as possible, thus requiring a very low dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure a solid design. If timing, startup, noise, PSRR, or any other transient specification is required, the design becomes more challenging. This section discusses the implementation and behavior of the LP2989 LDO.

### 9.2 Typical Application



\*Capacitance values shown are minimum required to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response. See the [Output Capacitor](#) section.

\*\*Shutdown must be actively terminated (see the [Shutdown Input Operation](#) section). Tie to INPUT (Pin4) if not use.

Figure 40. Typical Application Schematic

#### 9.2.1 Design Requirements

DESIGN PARAMETER	DESIGN REQUIREMENT
Input voltage	6.5 V, $\pm 10\%$ ,
Output voltage	5.0 V, $\pm 1\%$
Output current	500 mA (maximum), 1 mA (minimum)
RMS noise, 100 Hz to 100 kHz	18 $\mu$ VRMS typical
PSRR at 1 kHz	60 dB typical

## 9.2.2 Detailed Design Procedure

At 500-mA loading, the dropout of the LP2989 has 650-mV maximum dropout overtemperature, thus an 1500-mV headroom is sufficient for operation over both input and output voltage accuracy. The efficiency of the LP2989 in this configuration is  $V_{OUT} / V_{IN} = 76.9\%$ . To achieve the smallest form factor, the WSON package is selected. Input and output capacitors are selected in accordance with the capacitor recommendations. Ceramic capacitances of 2.2  $\mu\text{F}$  for the input and one 4.7- $\mu\text{F}$  capacitors for the output are selected. With an efficiency of 76.9% and a 500-mA maximum load, the internal power dissipation is 750 mW, which corresponds to a 26.1°C junction temperature rise for the WSON package. With an 85°C maximum ambient temperature, the junction temperature is at 111.1°C. To minimize noise, a bypass capacitance ( $C_{bypass}$ ) of 0.01  $\mu\text{F}$  is selected between pin 5 to pin 1 for LP2989.

### 9.2.2.1 LLP Package Devices

The LP2989 is offered in the 8-lead LLP surface mount package to allow for increased power dissipation compared to the SO-8 and Mini SO-8. For details on thermal performance as well as mounting and soldering specifications, refer to Application Note AN-1187.

For output voltages < 2 V, see LP2989LV ([SNVS806](#)) data sheet.

### 9.2.2.2 External Capacitors

Like any low-dropout regulator, the LP2989 requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

#### 9.2.2.2.1 Input Capacitor

An input capacitor whose size is at least 2.2  $\mu\text{F}$  is required between the LP2989 input and ground (the amount of capacitance may be increased without limit).

Characterization testing performed on the LP2989 has shown that if the amount of actual input capacitance drops below about 1.5  $\mu\text{F}$ , an unstable operating condition may result. Therefore, the next larger standard size (2.2  $\mu\text{F}$ ) is specified as the minimum required input capacitance. Capacitor tolerance and temperature variation must be considered when selecting a capacitor (see [Capacitor Characteristics](#) section) to assure the minimum requirement of 1.5  $\mu\text{F}$  is met over all operating conditions.

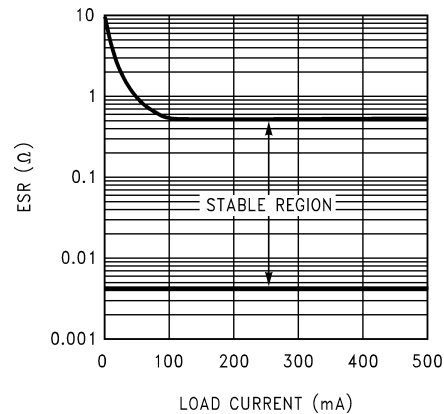
The input capacitor must be located at a distance of not more than 0.5 inches from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum may be used for this capacitor, assuming the minimum capacitance requirement is met.

#### 9.2.2.2.2 Output Capacitor

The LP2989 requires a ceramic output capacitor whose size is at least 4.7  $\mu\text{F}$ . The actual amount of capacitance on the output must never drop below about 3.5  $\mu\text{F}$  or unstable operation may result. For this reason, capacitance tolerance and temperature characteristics must be considered when selecting an output capacitor.

The LP2989 is designed specifically to work with ceramic output capacitors, using circuitry which allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 4 m $\Omega$ . It may also be possible to use Tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see the [Capacitor Characteristics](#) section).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (equivalent series resistance) value which is within the stable range. Curves are provided which show the stable ESR range as a function of load current (see [Figure 41](#)).



**Figure 41. Stable Region for Output Capacitor ESR**

**NOTE**

**Important:** The output capacitor must maintain its ESR within the stable region over the full operating temperature range of the application to assure stability.

It is important to remember that capacitor tolerance and variation with temperature must be considered when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. (See the [Capacitor Characteristics](#) section.)

The output capacitor must be located not more than 0.5" from the output pin and returned to a clean analog ground.

**9.2.2.2.3 Noise Bypass Capacitor**

Connecting a 10-nF capacitor to the Bypass pin significantly reduces noise on the regulator output. However, the capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few microamperes flowing in it, any significant loading on this node will cause a change in the regulated output voltage. For this reason, DC leakage current through the noise bypass capacitor must never exceed 100 nA, and should be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Ten-nF polypropylene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

**9.2.2.3 Capacitor Characteristics**

**9.2.2.3.1 Ceramic**

The LP2989 was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 4.7  $\mu$ F range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 4.7- $\mu$ F ceramic capacitor is in the range of 10 m $\Omega$  to 15 m $\Omega$ , which easily meets the ESR limits required for stability by the LP2989.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Many large-value ceramic capacitors ( $\geq 2.2 \mu$ F) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This could cause problems if a 4.7- $\mu$ F capacitor were used on the output because it will drop down to approximately 2.4  $\mu$ F at high ambient temperatures (which could cause the LP2989 to oscillate). Another significant problem with Z5U and Y5V dielectric devices is that the capacitance drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it.

**For these reasons, X7R and X5R type ceramic capacitors must be used on the input and output of the LP2989.**

#### 9.2.2.3.2 Tantalum

Tantalum capacitors are less desirable than ceramics for use as output capacitors because they are typically more expensive when comparing equivalent capacitance and voltage ratings in the 1  $\mu\text{F}$  to 4.7  $\mu\text{F}$  range.

Another important consideration is that Tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a Tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value.

It should also be noted that the ESR of a typical Tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

Tantalum capacitors may be used on the input as long as the requirement for minimum capacitance is met.

#### 9.2.2.3.3 Film

Polycarbonate and polypropylene film capacitors have excellent electrical performance: their ESR is the lowest of the three types listed, their capacitance is very stable with temperature, and DC leakage current is extremely low.

One disadvantage is that film capacitors are larger in physical size than ceramic or tantalum which makes film a poor choice for either input or output capacitors.

However, their low leakage makes them a good choice for the noise bypass capacitor. Because the required amount of capacitance is only 0.01  $\mu\text{F}$ , small surface-mount film capacitors are available in this size.

#### 9.2.2.4 Shutdown Input Operation

The LP2989 is shut off by driving the Shutdown input low, and turned on by pulling it high. If this feature is not to be used, the Shutdown input should be tied to  $V_{\text{IN}}$  to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the Shutdown input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the [Electrical Characteristics](#) table under VON/OFF.

To prevent mis-operation, the turn-on (and turn-off) voltage signals applied to the Shutdown input must have a slew rate which is  $\geq 40 \text{ mV}/\mu\text{s}$ .

#### CAUTION

The regulator output voltage **cannot** be guaranteed if a slow-moving AC (or DC) signal is applied that is in the range between the specified turn-on and turn-off voltages listed under the electrical specification  $V_{\text{ON/OFF}}$  (see the [Electrical Characteristics](#) table).

#### 9.2.2.5 Reverse Input-Output Voltage

The PNP power transistor used as the pass element in the LP2989 has an inherent diode connected between the regulator output and input.

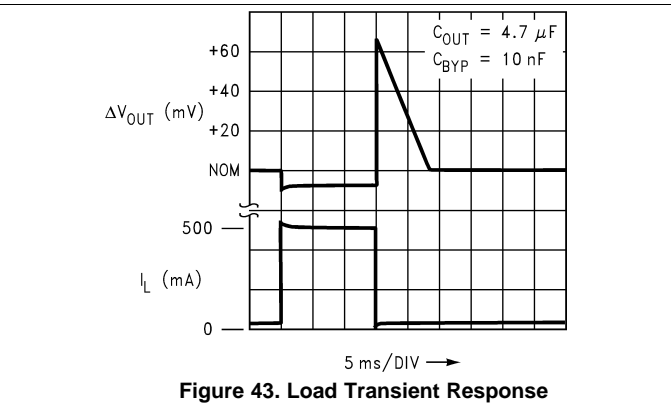
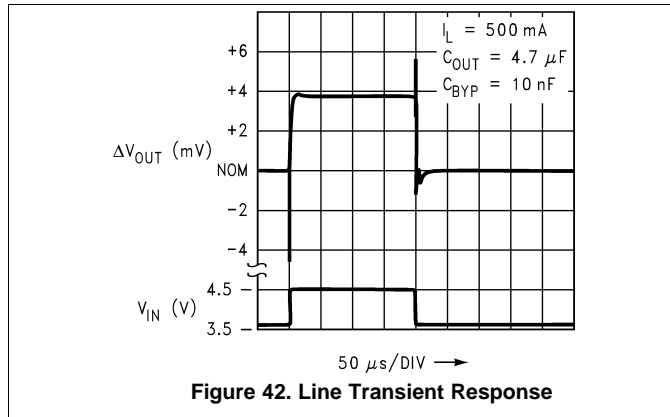
During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output is pulled above the input, this diode will turn on and current will flow into the regulator output.

In such cases, a parasitic SCR can latch which will allow high current to flow into  $V_{\text{IN}}$  can damage the part

In any application where the output may be pulled above the input, an external Schottky diode must be connected from  $V_{\text{IN}}$  to  $V_{\text{OUT}}$  (cathode on  $V_{\text{IN}}$ , anode on  $V_{\text{OUT}}$ ), to limit the reverse voltage across the LP2989 to 0.3 V (see the [Absolute Maximum Ratings](#) table).

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

The LP2989 is designed to operate from an input voltage supply range from 2.1 V to 16 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

## 11 Layout

### 11.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

## 11.2 Layout Example

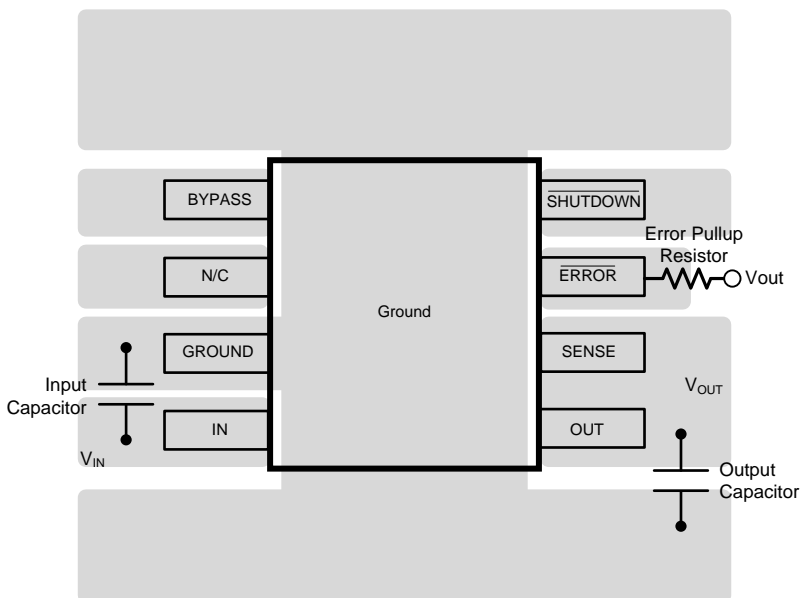


Figure 44. Layout Example

## 12 Device and Documentation Support

### 12.1 Trademarks

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### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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